REMARKS

The following Remarks are a full and complete response to the Office Action dated May 21, 2003. Claims 1, 3-6, 8-20, 22-25 and 27-39 are pending in this application. In the outstanding Office Action, the drawings were objected to; claims 4-6, 11-15, 23-25, 30-34 and 38-39 were rejected under 35 U.S.C. § 112, second paragraph; claim 38 was rejected under 35 U.S.C. § 102(b); and claims 38 and 39 were rejected under 35 U.S.C. § 103(a). Claims 1, 3, 8-10, 16-20, 22, 27-29, and 35-37 are allowed. No new matter has been added. Claims 4-6, 11-15, 23-25, 30-34 and 38-39 are presented for reconsideration.

Drawing Objections

The drawings were objected to under 37 C.F.R. § 1.83(a). The Office Action asserts that the drawings fail to show each and every feature of the invention recited in the claims.

Specifically, the Office Action asserts that the fourth transistor recited in claims 4-6 and 23-25 is not shown in the drawings. Transistor 30 illustrated in Figs. 8, 9, and 13-17 is one example of the recited fourth transistor. Accordingly the fourth transistor recited in claims 4-6 and 23-25 is illustrated in the drawings.

The Office Action also asserted that the drawings failed to show a fifth transistor as recited in claims 11 and 30. One example of the fifth transistor recited in claims 11 and 30 is illustrated in Figs. 9 and 15 as transistor 4. Accordingly, the fifth transistor recited in claims 11 and 30 is illustrated in the drawings.

The Office Action also asserts that the drawings failed to show a sixth transistor as recited in claims 12-13 and 31-32. One example of the sixth transistor recited in claims 12-13 and 31-32 is illustrated in Figs. 13 and 16 as transistor 50. Accordingly, it appears that the sixth transistor recited in claims 12-13 and 31-32 is shown in the drawings.

The specification at page 17, lines 24-28 also teaches that transistor 4 maybe inserted between the drains of the differential input transistors 1 and 2 in the embodiment shown in Fig. 11A.

The Office Action also asserts that the drawings fail to show a seventh transistor as recited in claims 14 and 33. Fig. 14 with transistor 60 shows one example of the seventh transistor recited in claims 14 and 33. Therefore, the seventh transistor recited in claims 14 and 15 is shown in the drawings.

The Office Action also asserts that the eighth transistor recited in claims 15 and 34 is not shown in the drawings. Transistor 70 shown in Fig. 17 is one example of the eighth transistor recited in claims 15 and 34. Therefore, the eighth transistor recited in claims 15 and 34 is shown in the drawings.

As discussed above, each claim element is shown in the drawings. Accordingly, Applicants request reconsideration and withdrawal of the objection of the drawings.

35 U.S.C. § 112, Second Paragraph

Claims 4-6, 11-15, 23-25, 30-34 and 38-39 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly

claim the subject matter which Applicant regards as the invention. Specifically, the Office Action asserts that these claims are misdescriptive because the circuits shown in the Figures and described in the specification do not specifically show the claimed circuits.

In determining the definiteness of claim language the Office Action must consider: the content of the application disclosure; the teachings of the prior art; and the claim interpretation that would be given by one possessing the ordinary skill in the art at the time the invention was made. To be definite, the claim must define the patentable subject matter with a reasonable degree of particularity and distinctness.

Even though the terms of the claim may appear to be definite, inconsistency with the specification or prior art teachings may make an otherwise definite claim take on an unreasonable degree of uncertainty.

The Office Action asserted that claims 4 and 23 were indefinite because the claims were misdescriptive. Claims 1 and 17 from which claims 4 and 23 depend read on Fig. 11A. An example of the third transistor is illustrated by transistor 30'. An example of the fourth transistor recited in claim 4 is illustrated by transistor 30 shown in Figs. 8-9, and 13-17. A person of ordinary skill in the art would understand that the addition of the fourth transistor in parallel to the third transistor could, for example, increase the drive current while reducing the impedance. Accordingly, claims 4-6 and 23-25 particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The Office Action asserts that claims 11 and 30 are misdescriptive because there is no single figure that discloses all of the elements of claim 11. As discussed above,

Figs. 9 and 15 illustrate transistor 4 which provides one example of the fifth transistor recited in claims 11 and 30. The present specification at page 16, line 7 indicates that Fig. 11A illustrates the third embodiment of the differential amplifier circuit. On page 17, lines 24-28 the specification states that transistor 4 may be inserted between the drains of the differential input transistors 1 and 2 in the third embodiment. Accordingly, claims 11 and 30 particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The Office Action also asserts that claims 12-13 and 31-32 are misdescriptive since there is no single figure which illustrates each element recited in these claims. As discussed above, Figs. 13 and 16 illustrate connecting a transistor 50 between the drains of the differential input transistors 1 and 2. The gate of transistor 50 is supplied with a high potential source voltage AVD. Since the specification at page 17, lines 24-28 specifically states inserting a transistor 4 which performs a similar function as transistor 50 in the embodiment shown in Fig. 11A, a person of ordinary skill in the art would understand that transistor 50 shown in Figs. 13 and 16 could be substituted for transistor 4. Accordingly, claims 12-13 and 31-32 particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The Office Action asserts that claims 14 and 33 are misdescriptive since Fig. 11A does not illustrate the seventh transistor recited in these claims. As discussed above, Fig. 14 with transistor 60 illustrates an example of the seventh transistor recited in claims 14 and 33. Based on the current specification and drawings a person of ordinary skill in the art would understand the scope of this claim. Accordingly, claims 14 and 33

particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The Office Action asserts that claims 15 and 34 are misdescriptive since no single figure illustrates all the elements recited in claims 15 and 34. As discussed above, Fig. 17 with transistor 70 illustrates one example of the eighth transistor recited in claims 15 and 34. Based on the current specification and drawings, one of ordinary skill in the art would understand the scope of claims 15 and 34. Accordingly, claims 15 and 34 particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claims 38 and 39 were rejected because the recitation of "said second power line" lacks antecedent basis. Claims 38 and 39 have been amended by replacing "said second power line" with "a second power line" to overcome the rejection of claims 38 and 39. Accordingly, claims 38 and 39 particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

As discussed above claims 4-6, 11-15, 23-25, 30-34 and 38-39 particularly point out and distinctly claim the subject matter which Applicants regards as the invention. Accordingly, Applicants request reconsideration and withdrawal of the rejection of claims 4-6, 11-15, 23-25, 30-34 and 38-39 under 35 U.S.C. § 112, second paragraph.

35 U.S.C. §§ 102(b) & 103(a)

Claim 38 was rejected under 35 U.S.C. § 102(b) as being anticipated by Branson (U.S. Patent No. 5,508,644). In making this rejection the Office Action asserts that this reference teaches each and every element of the claimed invention.

Claims 38 and 39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant Admitted Prior Art (Figure 7) in view of Branson (U.S. Patent No. 5,508,644). In making this rejection the Office Action asserts that the combination of these two references teach and/or suggest each and every element of the claimed invention. The Office Action also asserts that it would be obvious to one of ordinary skill in the art to combine these two references.

Claim 38 recites a differential amplifier circuit including a latch unit and a differential input portion. The differential input portion includes a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode. The control electrodes of the first and second transistors are supplied with a differential input signal. A third transistor for keeping a minute current to flow through the first and second transistors is inserted between a first power line and a common node to which the first electrodes of the first and second transistors are connected. A gate electrode of the third transistor receives a control signal of which level is changed in accordance with the operation of the differential amplifier circuit. An eighth transistor is inserted between a second power supply and the common node to which the first electrodes of the first and second transistors are connected. The control electrode of the eighth transistor is supplied with a fourth control signal. The third transistor doubles

as a transistor for supplying a drive current at the time the signal determination by the differential amplifier circuit.

Both claims 38 and 39 require that the gate electrode of the third transistor receives a control signal whose level changes in accordance with the operation of the differential amplifier circuit. In contrast, Branson provides a constant high power supply voltage V_{DD} to a gate of transistor 26. The Office Action considered the high power supply voltage V_{DD} to be the recited control signal. Thus, the "control signal" taught in Branson is a constant high power supply voltage. In contrast the recited control signal changes in accordance with the operation of the differential amplifier circuit.

Both claims 38 and 39 also recite that the third transistor doubles as a transistor for supplying a drive current at the time the signal determination by the differential amplifier circuit. Neither Figure 7 nor Branson teach and/or suggest a third transistor that keeps a minute current flowing through the first and second transistors and which doubles as a transistor for supplying a drive current at the time of signal determination by the differential amplifier circuit.

Accordingly neither Branson alone nor in combination with Figure 7 teaches and/or suggest the invention recited in claims 38-39. Specifically, these references fail to teach and/or suggest that the gate electrode of the third transistor receives a control signal of which level is changed in accordance of the operation of the differential amplifier circuit. The combination of these references also fails to disclose and/or suggest a third transistor which doubles as a transistor for supplying a drive current at the time of signal determination by the differential amplifier circuit. Accordingly, Applicants respectfully requests reconsideration and withdrawal of the rejection of claim

38 under 35 U.S.C. § 102(b) and the rejection of claims 38-39 under 35 U.S.C. § 103(a).

Conclusion

Applicants amendments and remarks have overcome the objections and rejections set forth in the Office Action dated May 21, 2003. Specifically, Applicants remarks have pointed out each feature of the invention specified in the claims in one of the figures and thus overcome the objection of the drawings under 37 C.F.R. § 1.83(a). Applicants remarks have demonstrated where claims 4-6, 11-15, 23-25 and 30-34 particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicants amendments to claims 38 and 39 correct the antecedent basis of these claims such that claims 38 and 39 now particularly point out the distinctly claimed subject matter which Applicant regards as the invention. Accordingly, Applicant has overcome the rejection of claims 4-6, 11-15, 23-25, 30-34 and 38-39 under 35 U.S.C. § 112, second paragraph. Applicants remarks have distinguish claim 38 from Branson and thus overcome the rejection of this claim under 35 U.S.C. § 102(b). Applicants remarks have also distinguish claims 38 and 39 from Figure 7 in combination with Branson, and thus overcome the rejection of these claims under 35 U.S.C. § 103(a). Accordingly, claims 4-6, 11-15, 23-25, 30-34 and 38-39 are in condition for allowance. Therefore, Applicants respectfully requests consideration and allowance of claims 4-6, 11-15, 23-25, 30-34 and 38-39. Claims 1, 3, 8-10, 16-20, 22, 27-29, and 35-37 are allowed.

Applicant submits that the application is now in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicant respectfully requests that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

In the event that any additional fees are due with respect to the filing of this paper, the undersigned authorizes the Office to charge any additional fees to our Deposit Account No. 01-2300, making reference to Docket No. 100021-00069

Respectfully submitted,

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